QUESTION #1

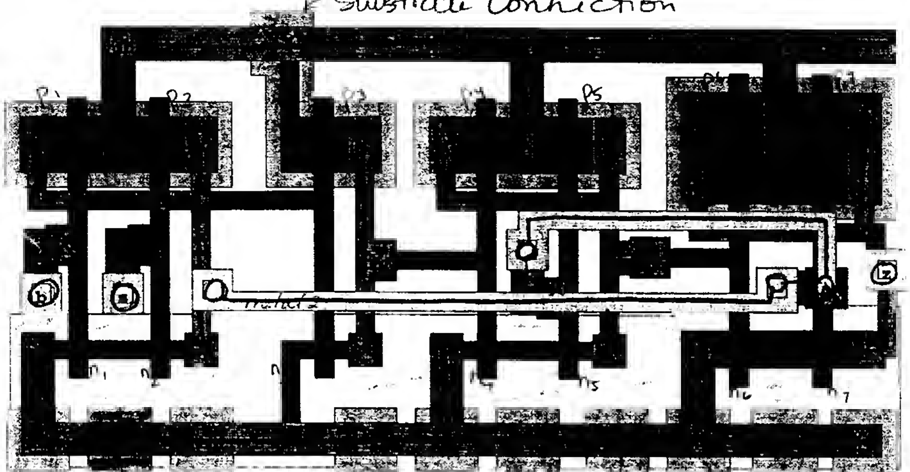
MARKS: 15 (5 + 5 + 5)

Being able to "reverse engineer" the layout of a facet (cell) is an important skill to verify the functionality of the cell as well as to uncover any layout errors. All the parts of this question relate to the diagram of the facet (cell) on the next page.

a) Identify the various layers by running coloured lines through the centre of each polygon (do not bother shading in the whole polygon as that will take too much of your time). Use red for polysilicon, blue for metal1, black for metal2, green for n+ diffusion, yellow/orange for p+ diffusion, "x" for contact cuts, and "o" for vias. If you need to use additional or different colours, make sure to provide a legend on your diagram.

Question #1 a) Work Sheet

Substrate Connection



Substrate connection

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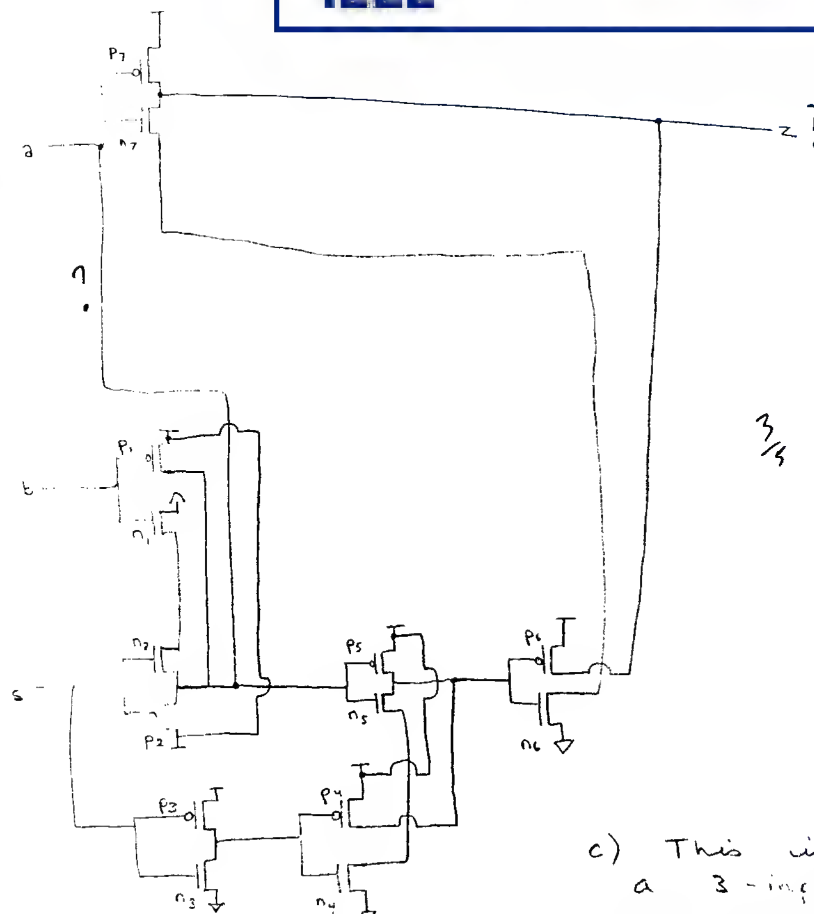
b) Draw the equivalent transis

c) What function does this cell



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c) This is a 3-input NAND Gate.

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QUESTION #2

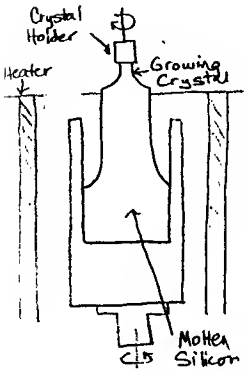
MARKS: 15 (5 + 5 + 5)

Consider the following three (3) parts of this question. For each of the parts, provide a short explanation. Do all three (3).

a) Describe the means whereby an ingot of silicon may be produced from a crucible melt of polycrystaline silicon. In particular, use a diagram and discuss the steps involved.

Question #2 a) Work Sheet

The Czochralski method is used to produce ingots of silicon from a crucible melt of polycrystalline silicon. The following steps are performed:



1) a crystal seed is held in a crystal holder
2) The seed is dipped into the melt to initiate single-crystal growth. The silicon is contained in a quartz crucible, surrounded by a graphite radiator. The atmosphere above the melt is helium or silicon

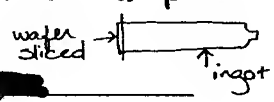
5/

3) The seed is gradually withdrawn from the melt, while being rotated.

4) As the crystal is withdrawn, it freezes in a perfect crystalline structure.

5) Growth continues for several hours. Growth rates are typically 30 to 180 mm/hr.

6) When all melt is consumed the ingot is sliced into wafers between 0.25mm + 1.0mm thick.



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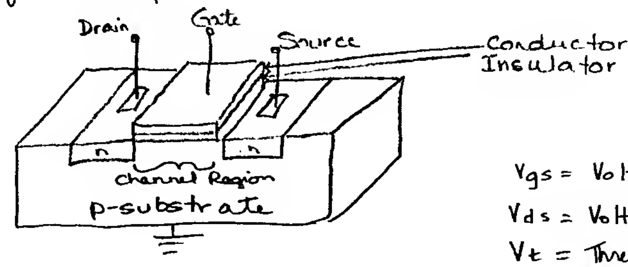
b) Describe the operation of an enhancement n-channel transistor. Use a diagram.

Question #2 b) Work Sheet

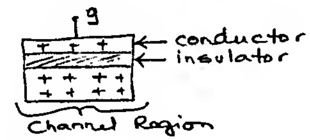
The following is an nMOS Enhancement Transistor:



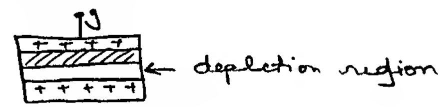
V_{gs} = Voltage Gate-Source
V_{ds} = Voltage Drain Source
V_t = Threshold Voltage

There are several main operation modes of the transistor:

When $V_{gs} << V_t$ this is the ACCUMULATION mode



When $V_{gs} = V_t$ this is the DEPLETION mode



when $V_{gs} > V_t$ this is the INVERSION mode

(over)

5/

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c) For a Medium Size Inverter (MSI) CMOS inverter, plot the output voltage vs input voltage characteristic for various selections of the input voltage. Where necessary, use device parameters as indicated on Page 2 of the examination paper.

Question #2 c) Work Sheet

Region A : $0 \le V_{in} \le V_{tn}$ $V_{out} = 5$ $I_{dsn} = -I_{dsp} = 0$

Region B : $V_t \le V_{in} < V_{DD}/2$ $0.7 \le V_{in} < 2.5$

$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in}-V_{tp})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right)V_{DD} - \frac{\beta_n}{\beta_p}(V_{in}-V_{tn})^2}$$

$\beta_n = \frac{\mu_n \epsilon}{t_{ox}}\left(\frac{W}{L}\right)$ $W = 3\mu m$, $L = 3\mu m$ $\mu_n = 775\ cm^2/Vs$ $t_{ox} = 5\times10^{-6}\ cm$ $\epsilon = (3.9)(8.8542\times10^{-14}\ F/cm)$

$= 5.3524\times10^{-5}\ F/Vs$

$\beta_p = \frac{\mu_p \epsilon}{t_{ox}}\left(\frac{W}{L}\right)$ $W = 9\mu m$, $L = 3\mu m$ $\mu_p = 250\ cm^2/Vs$ $\frac{\beta_n}{\beta_p} = 1.0333$

$= 5.1797\times10^{-5}\ F/Vs$

$V_{tp} = -0.8V$ $V_{tn} = 0.7V$ $V_{DD} = 5V$

$$V_{out} = (V_{in}+0.8) + \sqrt{(V_{in}+0.8)^2 - 2(V_{in} - 2.5 + 0.8)5 - 1.0333(V_{in}-0.7)^2}$$

V_{in}	V_{out}
1	
2	

A/5

Region C : $V_{in} = \frac{V_{DD}}{2}$ $V_{out} = \frac{V_{DD}}{2}$?

Region D : $V_{DD}/2 < V_{in} \le V_{DD} + V_{tp}$

$$V_{out} = (V_{in} - 0.7) - \sqrt{(V_{in}-0.7)^2 - 1.0333(V_{in} - 5 + 0.8)^2}$$

V_{in}	V_{out}
3	
4	

Region E : $V_{in} \ge V_{DD} - V_{tp}$ $V_{out} = 0$

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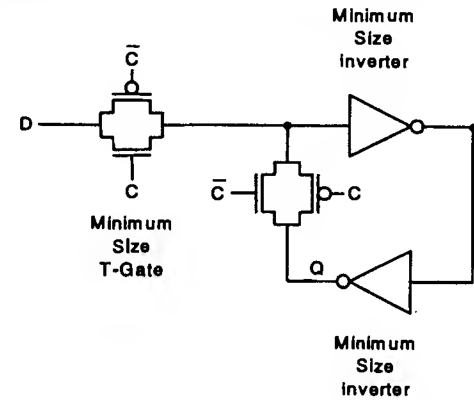
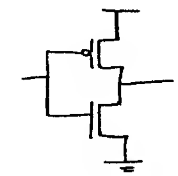
QUESTION #3

MARKS: 15 (5 + 10)

Consider the following circuit. It is the T-Latch that you analyzed as part of one of your assignments.

Note that a CMOS3DLM Minimum Size Inverter has a n-channel pull-down transistor of size 3μm:3μm (W:L) and a p-channel pull-up transistor of size 9μm:3μm (W:L). As well a CMOS3DLM Minimum Size T-Gate has a n-channel transistor of size 3μm:3μm (W:L) in parallel with a p-channel transistor of size 9μm:3μm (W:L).





[redacted]

"I can't take it anymore, Felix. I'm crackin' up. Everything you do irritates me. And when you're not here, the things I know you're *gonna* do when you come in irritate me. You leave me little notes on my pillow. I told you 158 times I cannot stand little notes on my pillow! 'We are all out of cornflakes. F.U.' It took me three hours to figure out that F.U. was Felix Unger."

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a) How much faster (or slower) is a Minimum Size Inverter and T-Gate series combination compared to just a Minimum Size Inverter? Assume the circuit driving each is a Minimum Size Inverter. Assume the load on each is a Minimum Size Inverter.

Question #3 a) Work Sheet

Timing dependent on gate area

Gate area of a MSI $= 3\times 3\ \mu m^2 + 9\times 3\ \mu m^2$
$= 36\ \mu m^2$

? Gate area of a T-Gate $= 3\times 3\ \mu m^2 + 9\times 3\ \mu m^2$
$= 36\ \mu m^2$

MSI + TGate + MSI load Area $= 3\,(36\ \mu m^2) = 108\ \mu m^2$

MSI + MSI load $= 2\,(36\ \mu m^2) = 72\ \mu m^2$

$\therefore$ MSI + TGate is faster by $\frac{108}{72} = 1.5$ times.

$R_{MSI} + R_{TGATE} = ?$ $\therefore$ SLOWER.

C_L SAME IN BOTH CASES.

$R_{MSI} = ?$

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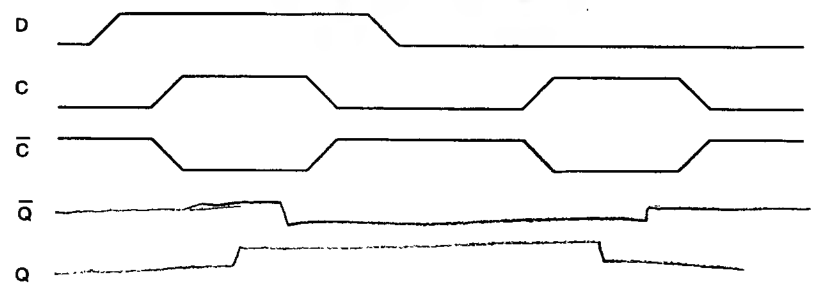
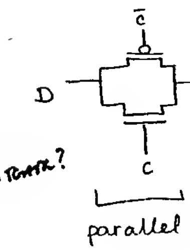
b) Draw a timing diagram for the T-Latch circuit. Use the inputs as shown below (illustrative only; not to scale). Calculate and indicate important times (delays and rise/fall times).

Assume the following (you may also make other appropriate assumptions):

- Assume 2ns rise and fall times of the C input.
- Assume the D input has stabilized before the clock inputs are asserted.
- Assume that the only load capacitances are the gate capacitances of the transistors.
- Assume 10%-90% (90%-10%) rise (fall) times are the same as the 0%-100% (100%-0%) rise (fall) times.

Question #3 b) Work Sheet





R_{TGATE}?

$\beta_{eff} = \beta_n + \beta_p = (5.3524\times 10^{-5} + 5.1797\times 10^{-5})\ F/Vs$
$= 1.053\times 10^{-4}\ F/Vs$

$t_F = \frac{A_N C_L}{\beta_N}$ $A_N = (3\times 3 + 9\times 3)\ \mu m^2 = 36\ \mu m^2$

$C_L = C_N + C_P = \frac{\epsilon A}{t_{ox}} = \frac{\epsilon L W}{t_{ox}} = \frac{\epsilon L(W_p + W_n)}{t_{ox}}$

$= \frac{3.9(8.854\times 10^{-14})(3\times 10^{-4})(9\times 10^{-4} + 3\times 10^{-4})}{5\times 10^{-6}}$

$= 24.86\times 10^{-15}\ F$

$t_F = \frac{(9\times 10^{-6})(24.86\times 10^{-15})}{5.3524\times 10^{-5}}$
$= 4.18\times 10^{-21}\ s$

$\frac{1}{\beta_{eff}} = \frac{1}{5.3524\times 10^{-5}} + \frac{1}{5.1797\times 10^{-5}}$ $\beta_{eff} = 2.632\times 10^{-5}\ F/V$

$t_F = 36\ \mu m^2$ $\frac{1}{C_L} = \frac{1}{C_N} + \frac{1}{C_P} = \frac{t_{ox}}{\epsilon L W_n} + \frac{t_{ox}}{\epsilon L W_n}$

$C_L = 4.66\times 10^{-15}\ F$ $t_F = \frac{(9\cdot 10^{-6})(4.66\times 10^{-15})}{5.3524\times 10^{-5}}$
$= 7.836\times 10^{-22}\ s$

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** More work on back of pg. 8